The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-21 (Previously Cancelled).

22. (Previously Presented) A current source circuit comprising:

a first PMOS transistor having a source coupled to a first power source, a gate receiving a voltage from a voltage circuit, and a drain coupled to a node; and

a compensation circuit comprising;

more than one compensation PMOS transistors, each compensation PMOS transistor having a gate, a source coupled to the first power source, and a drain coupled to the node; and

more than one subtracter, each subtracter coupled to the gate of each compensation PMOS transistor, each subtracter configured to supply voltage expressed by arithmetic series a_k to the gate of each compensation PMOS transistor,

where the a_k is the arithmetic series equal to :

$V_{g1} - kV_{d1}$ (k=1, 2, . . ., n),

V_{d1} is the drain-source voltage of the first transistor,

V_{g1} is the gate-source voltage of the first transistor, and

n is the number of the PMOS transistors of the compensation circuit.

23. (Currently Amended) A current source circuit comprising:

a first PMOS transistor group having at least two PMOS transistors connected in series, the first PMOS transistor group including:

a first PMOS transistor having a source coupled to a first power source, a gate receiving a first voltage provided by a voltage circuit, and a drain, wherein the first PMOS transistor is defined as being the electrically closest to the first power source,

a second PMOS transistor having a source, a gate receiving a second voltage provided by a the voltage circuit, and a drain wherein the drain of the second PMOS transistor coupled to a node, wherein the last PMOS transistors is defined as being the electrically furthest from the first power source; and

a compensation circuit comprising a second PMOS transistor group having at least two PMOS transistors connected in series, the second PMOS transistor group including:

a third PMOS transistor having a gate, a source, and a drain, wherein the source of the third PMOS transistor is coupled to the first power source, wherein the third PMOS transistor is defined as being the electrically closest to the first power source in the second PMOS transistor group, and

a fourth PMOS transistor having a gate, a source, and a drain, wherein the drain of the fourth PMOS transistor is coupled to the node, wherein the fourth PMOS transistor is defined as being the electrically furthest from the first power source in the second transistor group; and

the group of subtracters, each subtracter, including:

a first subtracter coupled to a gate of the third PMOS transistor, the first subtracter configured to supply difference voltages, being a difference between gate-source voltages and drain-source voltage of the first PMOS transistor, to the gate source of the third PMOS transistor;

a second subtracter coupled to a gate of the fourth PMOS transistor, the second subtracter configured to supply difference voltages, being a difference between gate-source voltages and drain-source voltage of the second PMOS transistor, to the gate source of the third PMOS transistor.

24. (New) A current source circuit comprising:

a first PMOS transistor group having at least two PMOS transistors connected in series, the first PMOS transistor group including:

a first PMOS transistor having a source coupled to a first power source, a gate receiving a first voltage provided by a first voltage circuit, and a drain, wherein the first PMOS transistor is defined as being the electrically closest to the first power source,

a second PMOS transistor having a source, a gate receiving a second voltage provided by a second voltage circuit, and a drain wherein the drain of the second PMOS transistor coupled to a node, wherein the last PMOS transistors is defined as being the electrically furthest from the first power source; and

a compensation circuit comprising a second PMOS transistor group having at least two PMOS transistors connected in series, the second PMOS transistor group including:

a third PMOS transistor having a gate, a source, and a drain, wherein the source of the third PMOS transistor is coupled to the first power source, wherein the third PMOS transistor is defined as

being the electrically closest to the first power source in the second PMOS transistor group, and

a fourth PMOS transistor having a gate, a source, and a drain, wherein the drain of the fourth PMOS transistor is coupled to the node, wherein the fourth PMOS transistor is defined as being the electrically furthest from the first power source in the second transistor group; and

the group of subtracters, each subtracter, including:

a first subtracter coupled to a gate of the third PMOS transistor, the first subtracter configured to supply difference voltages, being a difference between gate-source voltages and drain-source voltage of the first PMOS transistor, to the gate source of the third PMOS transistor;

a second subtracter coupled to a gate of the fourth PMOS transistor, the second subtracter configured to supply difference voltages, being a difference between gate-source voltages and drain-source voltage of the second PMOS transistor, to the gate source of the third PMOS transistor.